Amendments to the Claims:

1-10. (canceled)

11. (Previously Presented) A method of processing data comprising:

receiving through multiple serial transmission channels multiple streams of serial data including predefined bit patterns being transmitted from remote sources;

generating from each one of the multiple stream of serial data a group of parallel bits including the predefined bit patterns;

storing in a computer memory the parallel bits including the predefined bit patterns;

searching the memory with a programmed computer to detect the predefined bit patterns received and stored in each of said different groups;

measuring misalignment between at least two groups of predefined bit patterns; and

using said programmed computer and the misalignment measurement to adjust the predefined bit patterns between selected ones of said groups until said predefined bit patterns are linearly aligned within said computer memory.

12. (Previously Presented) The method of claim 11 wherein the predefined bit pattern includes 0101.

13. (Previously Presented) An apparatus comprising:

N data recovery systems, wherein N > 2 and each one of the data recovery systems being operable to receive a serial data stream, including predefined bit patterns transmitted from remote source, from a different communication channel and to generate parallel data streams including the predefined bit patterns therefrom; and

an aligner operatively coupled to the N data recovery systems; said aligner being operable to receive the parallel data streams, determine misalignment between the predefined bit patterns associated with groups of bits in different parallel data streams and to adjust the predefined bit patterns between the different parallel data streams relative to one another to remove the misalignment therebetween.

14. (Previously Presented) The apparatus of claim 13 further including a transmitting subsystem for generating the N serial data streams.

15. (Previously Presented) The apparatus of claim 14 further including a high speed bus formed from a plurality of different serially communication channel operatively coupling the transmitting sub-system to the N data recovery systems.

16. (Previously Presented) The apparatus of claim 13 wherein each of the N data recovery systems includes a receiver circuit; and

a nibble recovery circuit operatively coupled to generate one of the parallel data streams.

17. (Previously Presented) The apparatus of claim 13 wherein the aligner includes M groups of multiple storage devices arranged in parallel; wherein $M \geq 2$;

P multiplexers wherein each one of the P multiplexers is operatively coupled to one of the M groups of multiple storage devices; and

a controller that generates control signals that drive each one of the multiplexer to select and output data from one of the coupled multiple storage devices.

18. (Previously Presented) The apparatus of claim 17 further including a memory operatively coupled to outputs of the P multiplexers and a controller operatively coupled to the memory.

19. (Previously Presented) The apparatus of claim 18 wherein each one of the multiple storage devices includes a plurality of serially connected multi-bit latches.

20. (Currently Amended) A circuit arrangement to align groups of data bits comprising:

M parallel sets of multiple storage devices wherein each set of the multiple storage devices includes N serially coupled latches operable to store bits representing portions of a word;

P multiplexers, wherein each of the P multiplexers is operatively connected to a set of the M parallel sets of multiple storage devices;

P word alignment select lines, wherein each of the P word alignment select lines is operatively coupled to one of the P multiplexers;

a memory operatively connected to the P multiplexers, said memory being operable to store the groups of bits outputted from said multiplexers; and

a controller operatively connected to determine the ~~orientation~~ location of ~~data~~ a predefined bit pattern in the memory and generate control signals on the P word alignment select lines that causes the multiplexers to select storage devices in each of the M parallel sets of multiple storage devices so that data from the selected storage devices are arranged in a predefined orientation within said memory.

21. (Previously Presented) The circuit arrangement of claim 20 wherein the controller includes a processor executing a program.

22. (Previously Presented) The circuit arrangement of claim 21 wherein M = 4.

23. (Previously Presented) The circuit arrangement of claim 20 wherein the predefined orientation is linear.

24. (previously presented) The method of claim 11 wherein bits in each group represents portion of a word.

25. (Currently Amended) A method of processing data comprising the acts of:

receiving multiple streams of serial data transmitted from remote source through multiple serial channels;

generating from each one of the multiple stream of serial data a group of parallel bit streams including predefined bit patterns transmitted from the remote ~~remove~~ source;

storing in a computer memory the group of parallel bit streams including the predefined bit pattern generated for each one of serial bit stream;

searching the memory with a programmed computer to detect the predefined bit pattern received and stored in each of said different groups;

measuring misalignment between at least two groups of predefined bit patterns, so found; and

using said programmed computer and the misalignment measurement to adjust the predefined bit pattern between selected ones of said groups until said bit patterns are linearly aligned within said computer memory.

26. (Currently Amended) The method of ~~claim 1~~ claim 11 wherein the misalignment includes offset between the at least two groups of predefined bit patterns.

27. (New) The circuit arrangement of claim 20 wherein N = 3.